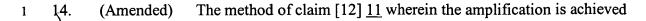
In the claims:

		Flease amend the claims indicated below.
1	1.	(Amended) A computer system comprising:
2	\	a processor including:
3		a central processing unit (CPU) core to execute non-graphic instructions;
4		a graphics core to compute graphical transformations via supersampling
5		techniques; and
6		a unified graphics cache coupled to the graphics core, wherein the unified
1		graphics cache stores texture data, color data and depth data.
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1	2.	(Unchanged) The computer system of claim 1 wherein the graphics cache
2		comprises:
3		a texture cache to store texture data; and
4		a color and depth buffer to store the color data and the depth data.
1	3.	(Amended) The computer system of claim 1 further comprising:
2		[a central processing unit (CPU) core; and]
3		a CPU cache coupled to the CPU core.
_	4	
1	4.	(Unchanged) The computer system of claim 3 further comprising a bus interface
2		coupled to the CPU cache and the graphics cache.
1	5.	(Amended) The computer system of claim 1 wherein the graphics core
2		[operates] performs rendering according to a tile-based rendering architecture.
1	6.	(Amended) The computer system of claim 1 further comprising:

- a bus interface coupled to CPU cache and the graphics cache; and
- a main memory coupled to the bus interface.
- 1 7. (Unchanged) The computer system of claim 2 wherein the graphics core
- 2 amplifies image polygons and renders the polygons into the graphics cache.
- 1 8. (Amended) The computer system of claim 7 wherein [the] amplification of the
- 2 image polygons are implemented via viewport transformation.
- 9. (Unchanged) The computer system of claim 7 wherein the graphics core downsamples the image polygons after the polygons have been rendered.
- 1 10. (Unchanged) The computer system of claim 9 wherein the downsampling of the
- 2 image polygons are implemented by executing a bit aligned block transfer.
- 1 11. (Amended) A method for supersampling an image comprising:
- receiving polygons of a first tile of the image at a graphics core; and
- amplifying the polygons at the graphics core;
- rendering the polygons of the first tile into a unified graphics cache, wherein the
- 5 unified graphics cache stores texture data, color data and depth data of the image.
- 1 12. (Amended) The method of claim 11 further comprising [amplifying the
- 2 polygons after receiving polygons] executing a stretch aligned block transfer at the
- 3 graphics core after rendering the polygons.
- 1 13. (Amended) The method of claim [12] 11 wherein the polygons are amplified
- 2 four times the original size of the image.



- 2 using viewport transformation.
- 1 15. (Unchanged) The method of claim 11 wherein the process of rendering the
- 2 polygons comprises:
- 3 setting up the image polygons; and
- rasterizing pixels within the image polygons.
 - 16. (Unchanged) The method of claim 15 further comprising texturing the pixels
- within the image polygons.
- 1 17. (Unchanged) The method of claim 11 further comprising downsampling the
- 2 polygons after the polygons have been rendered.
- 1 18. (Unchanged) The method of claim 17 wherein the downsampling is achieved by
- 2 executing a bit aligned block transfer.
- 1 19. (Unchanged) The method of claim 11 further comprising:
- determining whether the unified graphics cache includes more tiles that are to be
- 3 rendered; and
- if so, receiving polygons of a second the of the image at the graphics core; and
- rendering the polygons of the second tile into the unified graphics cache.
- 1 20. (Amended) A central processing unit (CPU) comprising:
- 2 a CPU core to execute non-graphic instructions;
- 3 CPU cache coupled to the CPU core;

4	a graphics accelerator to compute graphical transformations via supersampling
	7 .

- 5 <u>techniques</u>; and
- a unified graphics cache coupled to the graphics core and the CPU, [wherein the
- 7 unified graphics cache stores] to store texture data, color data and depth data.
- 1 21. (Unchanged) The CPU of claim 20 wherein the graphics cache comprises:
- 2 a texture cache to store texture data; and
- a color and depth suffer to store the color data and the depth data.
- 22. (Amended) The CPU of claim 20 wherein the graphics core amplifies image
- 2 polygons and renders the polygons into the graphics cache. [further comprising:
- a CPU core; and
- a CPU cache coupled to the CPU core.]
- 1 23. (Unchanged) The CPU of claim 22 further comprising a bus interface coupled to
- 2 the CPU cache and the graphics cache.
- 1 24. (Amended) The CPU of claim 23 wherein the graphics accelerator [operates]
- 2 <u>performs rendering</u> according to a tile-based rendering architecture.